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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/826,179	04/04/2001	Keisuke Goto	KPM-01501	2868

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EXAMINER

LE, DINH THANH

ART UNIT PAPER NUMBER

2816

DATE MAILED: 05/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/826,179

Applicant(s)

GOTO ET AL.

Examiner

DINH T. LE

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 March 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 and 17-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 17-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

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FINAL REJECTION

Response to Applicant's Amendment

The rejection under 35USC 112, second paragraph, is withdrawn in view of the amendments to the claims

Claims Rejections

Claim Rejections - 35 USC § 112

Claims 1-9 and 17-24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. It is not understood how the delay time of the first delay section as recited in claims 1 and 17 and the delay time of the second section as recited in claim 7 can be dependent and independent from the frequency since the specification does not show the detailed structure of these delay sections and shows how the delay time can be dependent and independent from the frequency. As understood, the delay time of a delay element is always depending on an operational frequency. Clarification is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 7, 8, 9, 17-19 and 23 are rejected under 35 USC 102 (e) as being anticipated by Shibayama (US 6,111,448).

Figures 1, 10 and 13 of Shibayama shows a DLL circuit comprising a first variable delay section (12a) with a frequency dependent delay time since the delay time of the delay is inherently depending upon the operating frequency, a second delay section (13a) with a fixed delay time, a phase detector (12b) and a controller (12c).

Claims 1-2, 17-19 and 23 are further rejected under 35 USC 102 (b) as being anticipated by Jefferson (US 5,642,082).

Figures 1 and 4-7 of Jefferson shows a DLL circuit comprising a first variable delay section (18,) with a frequency dependent delay time since the delay time of the delay is depending upon the operating frequency, see column 2, lines 30-36, a second delay section (20) with a fixed delay time, a phase detector (12) and a controller (14, 16).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-9 and 17-23 are rejected under 35 USC 103 (a) as being unpatentable over Figure 9 of

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the applicant's admitted prior art in view Shibayama (US 6,111,448).

With regard to claims 1-3, 6-9, 17, 18, 19 and 22-23, Figure 9 of the admitted prior art shows a DLL circuit comprising a first variable delay section (311) with a frequency dependent delay time, a phase detector (313) and a controller (312) but does not show the second delay section having a plurality of delay elements. Shibayama teaches a DLL in Figure 14 comprising a fixed delay inverters (13) for providing a plurality of output clock signals. It would have been obvious to a person having skill in the art at the time the invention was made to place the delay inverters taught by Jefferson after the variable delay section of the admitted prior art for the purpose of providing a plurality of output clock signals.

With regard to claims 4-5 and 20-21, as well known in the art, the time delay of the inverter is selectable by selecting the threshold voltage of the inverter. Thus, selecting the delay time for the inverter for a particular applications would have been obvious and is considered to be a matter of a design expedient for an engineer.

Claims 24 is rejected under 35 USC 103 (a) as being unpatentable over Figure 1 of the admitted prior art in view of Figure 9 of the admitted prior art and Shibayama (US 6,111,448).

Figure 1 of the admitted prior art shows a circuit comprising a DLL coupled to a memory section but does not disclose that the DLL comprising the first delay section and the fixed delay section. Figure 9 of the admitted prior art in view of Shibayama teaches a DLL circuit as discussed above for the purpose of generating a plurality of output clock signals. It would have been obvious to a person having skill in the art at the time the invention was made to employ the

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modified DLL taught by Figure 9 of the admitted prior art in view of Shibayama in the circuit of Figure 1 of the admitted prior art for the purpose of providing a plurality of output clock signals.

Claims 4-6 and 20-22 are rejected under 35 USC 103 (a) as being unpatentable over Shibayama (US 6,111,448).

Figures 10 and 13-14 of Shibayama discloses a DLL with all of the limitations of the claimed invention as discussed above but does not disclose that, i.e., the delay elements having substantially a same delay time or a different delay time. However, as understood by a person skill in the art, the delay elements (13a-13j) of Shibayama can be selectable to provide different delay times depending upon an application. Thus, selecting the delay elements is a common practice for an engineer and is considered to be a matter of a design expedient for the engineer. Lacking of showing any criticality, a skilled artisan would have been obvious to select the delay time of the delay elements of Shibayama for the purpose of accommodating with a selected system.

Claim 24 is rejected under 35 USC 103 (a) as being unpatentable over Figure 1 of the admitted in view of Shibayama (US 6,111,448).

Figure 1 of the admitted prior art shows a circuit comprising a DLL coupled to a memory section but does not disclose that the DLL comprises the first delay section and the fixed delay section. Figures 10 and 13-14 of Shibayama teaches a DLL circuit as discussed above for the purpose of generating a plurality of output clock signals with low skew, see column 2, lines 47-50. It would have been obvious to a person having skill in the art at the time the invention was

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made to employ the DLL taught by Shibayama in the circuit of Figure 1 of the admitted prior art for the purpose of providing a plurality of output clock signals with low skew.

Response to Applicant's Arguments

The applicant argues that the delay time of the variable delay section in the Shibayama reference is not depending on frequency. The argument is not persuasive because the delay time of the first variable delay section (12a) of Shibayama is inherently depending upon the operating frequency because, as well known in the art, the delay time of a delay element is always change with the operating frequency. See how this limitation being taught in column 2, lines 30-36 of the Jefferson reference.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Dinh Le whose telephone number is (703) 305-3790.

The examiner can normally be reached on Monday to Friday from 7:00 A.M. to 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-7725.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

May 9, 2003

DINH LE
Primary Examiner

A handwritten signature in black ink, appearing to read 'Dinh Le', written over the printed name and title.